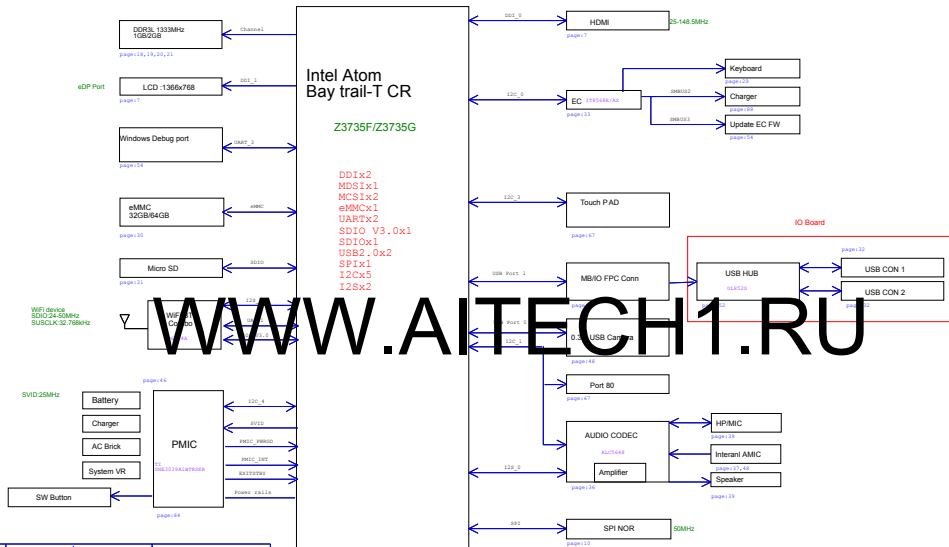


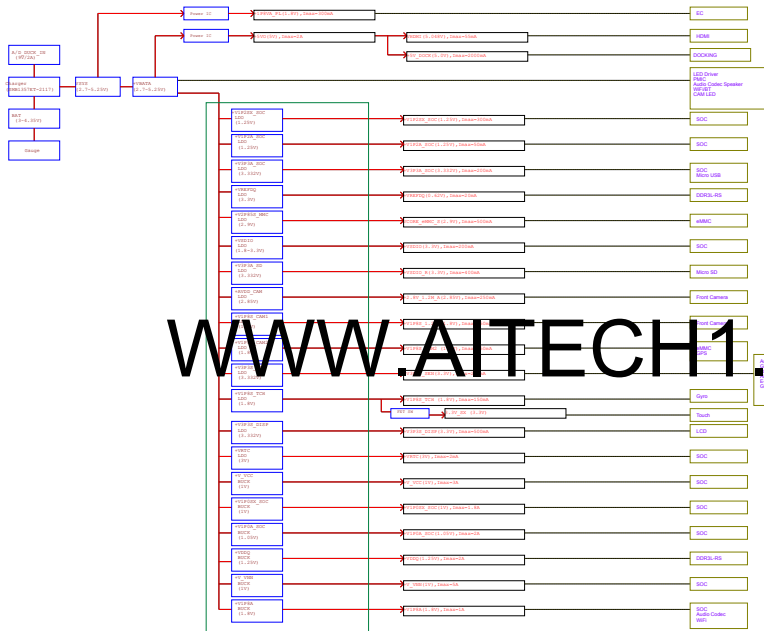
X205TA Block Diagram

2014_1218_1530



I2C Bus	Device	PART	7-bit Address	Max Operation Frequency
I2C_0	9C	19574687A0		
I2C_1				
	Audio	AC15448		
I2C_2				
I2C_3	59			
I2C_4	98C	88E3336A1879000	0066	

Q2: 19.2/25MHz
 Q2: 100MHz - 400kHz, 1MHz, 1.7MHz
 platform CLK: 19.2MHz



PMIC



4.5.1 Voltage Regulator Default Voltage

The following table is a list of the default on rails.

Table 4-3: Standby Power Rail Defaults

Voltage Regulator	Rail Function	Sleep State based on SLP50IXS pin
Buck 1	VCC	On
Buck 2	VNN (CHT), V1P05X (BYT)	BYT(Off), CHT(On) – device configuration Reduced voltage based on BUCK2VSLEEP setting
Buck 3	V1P0/V1P05/V1P15	On Reduced voltage based on BUCK3VSLEEP setting
Buck 4	VDDQ	On
Buck 5	VNN (BYT), VSG (CHT)	BYT(On), CHT(Off) – device configuration Reduced voltage based on BUCK5VSLEEP setting
Buck 6	V1P8	On
LD01	V1P25X (BYT), V1P2A (CHT)	BYT(Off), CHT(On)
LD02	V1P2A (BYT)	On
LD03	V3P3A	On
LD04	VRTC	On
LD05	VREFDQ	On
LD06	eMMC	On
All other rails are controlled by the driver		Based on register control from the driver

4.5.1.2 Dollar Cove based PMIC

Table 4-61: Bay Trail-F (Entry Type 7) Platform Voltage Rails ON/OFF at Various Power States (Sheet 1 of 2)

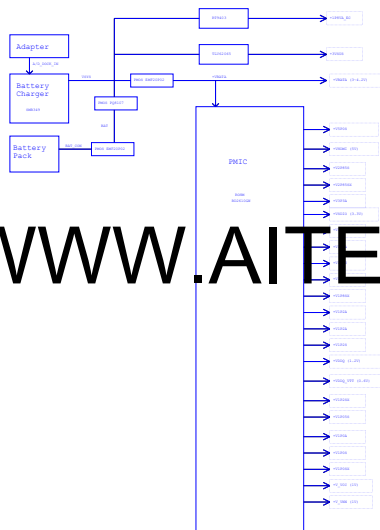
#	Voltage Rail	On	Stuck	Off
1	+V1P05X	On	On	Off
2	+V1P05X	On	On	Off
3	+V1P05X	On	On	Off
4	+V1P05X	On	On	Off
5	+V1P05X	On	On	Off
6	+V1P05X	On	On	Off
7	+V1P05X	On	On	Off
8	+V1P05X	On	On	Off
9	+V1P05X	On	On	Off
10	+V1P05X	On	On	Off
11	+V1P05X	On	On	Off
12	+V1P05X	On	On	Off
13	+V1P05X	On	On	Off
14	+V1P05X	On	On	Off
15	+V1P05X	On	On	Off
16	+V1P05X	On	On	Off

Table 4-61: Bay Trail-F (Entry Type 3) Platform Voltage Rails ON/OFF at Various Power States (Sheet 2 of 2)

#	Voltage Rail	On	Stuck	Off
17	+V1P05X	On	On	Off
18	+V1P05X	On	On	Off
19	+V1P05X	On	On	Off

Note: On/Off means the status of these rails are based on register control from the driver.

T100VC Power Map

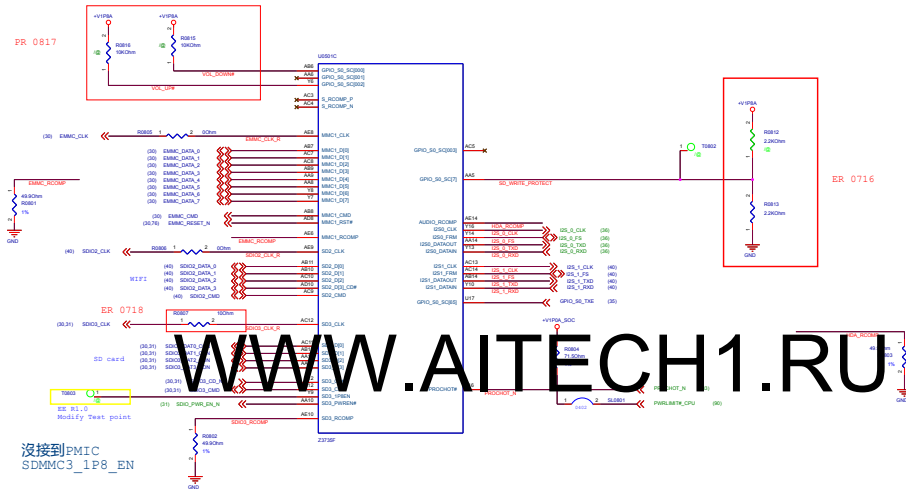


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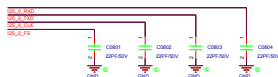


		Title : BAY DRAM1	
ASUSTek COMPUTER INC. EFRD		Engineer: EE3 RD	
Size	Project Name X20STA	Rev	
Date: Thursday, December 19, 2014		Page 5 of 29	

PR 0817



沒接到PMIC
SDMMC3_1P8_EN



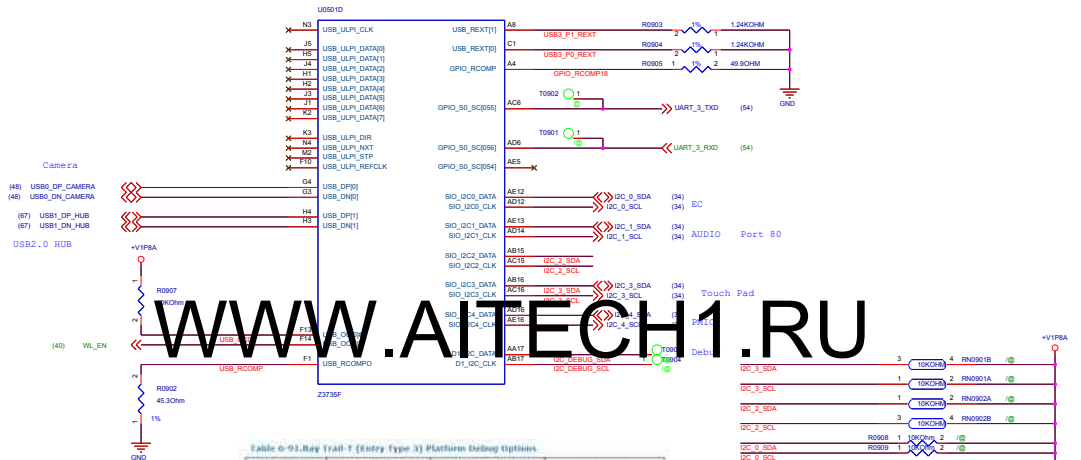
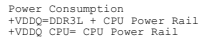
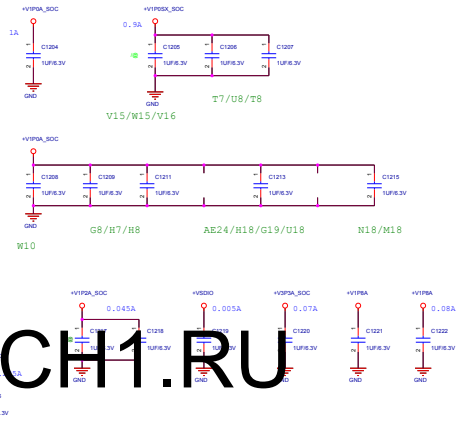
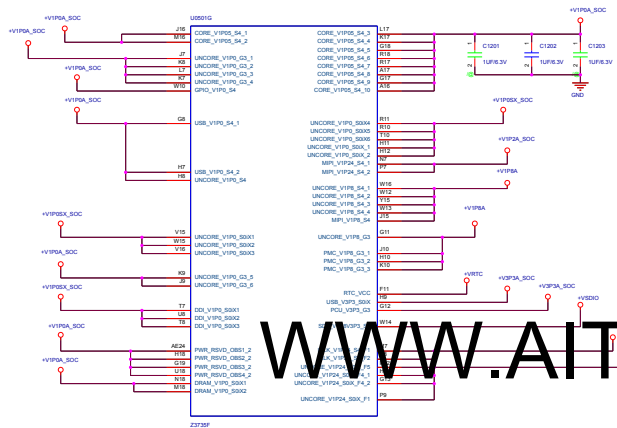


Table 6-91.Bay Trail-T (Entry Type 3) Platform Debug Options

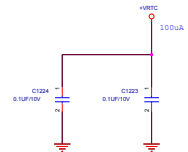
Debugged Element	Tool	Hardware Port	Connector
BIOS Source Debug	ITP II, Green Hubs, Arrium Lauterbach	Primary JTAG	VD460 (Debug Card)
Android OS	ADB	USB2 ports and UART3/COM3	USB2 Port1 (Debug Card or Native USB port)
SW Trace -Afterstate	Terminal Port BU Display	UART3/COM3	USB COM (Debug Card)
TxE, Rx, RxC	Various	Primary JTAG	VD460 (Debug Card)
TxE Trace	TBT	D1_I2C port	I2C (Debug Card)
SPI-IOV4 Programming Header	Dev-Prog. FET	SPE Programming Header	8 pin (Debug Card)
SDX, Power Sequencing	PETs-Platform Evaluation Test System	PETs Interface	19 Pin Connector (Debug Card)
I2C peripherals	External I2C Analyzer	Test Points on all I2C SCL, SDA Signals	Test Points (Board)

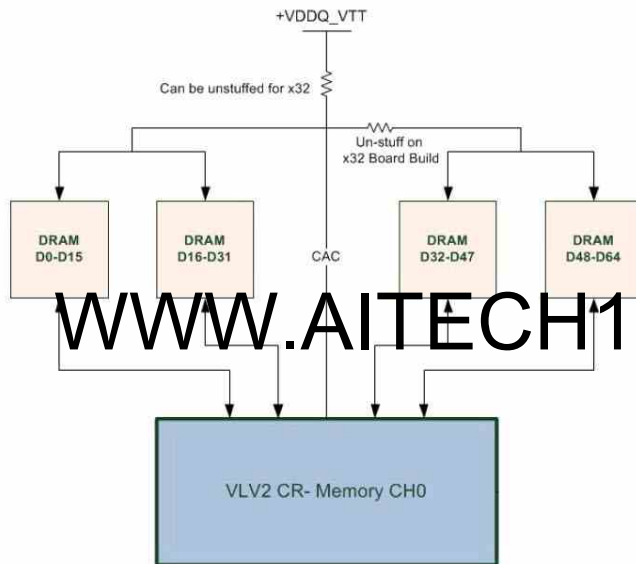






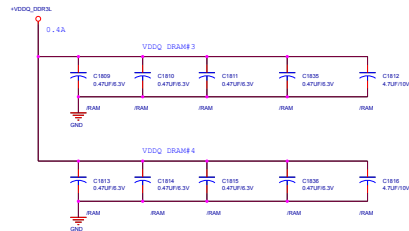
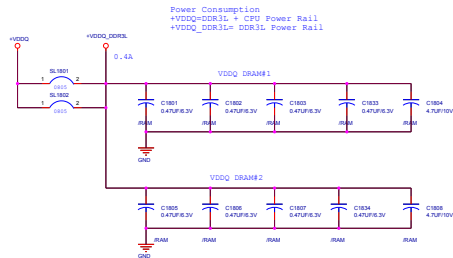
WWW.AITECH1.RU



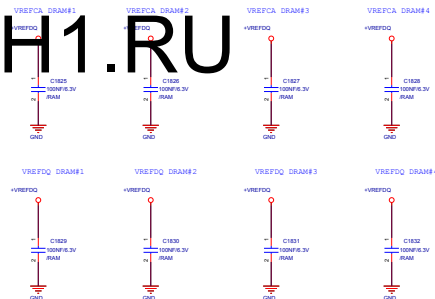
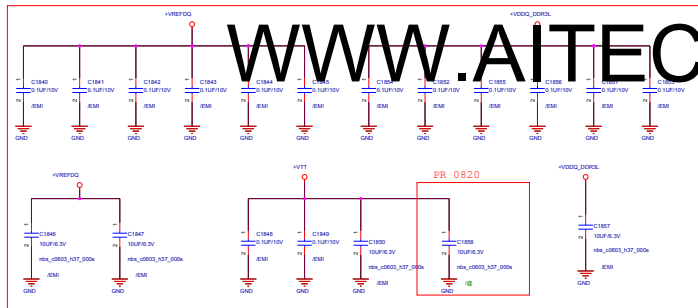


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ASUS		Title : 17.DDR3L(1)	
ASUSTek COMPUTER INC. EPAD		Engineer: EE3 RD	
Size A	Project Name X205TA	Rev 2.1	
Date: Thursday, December 18, 2014		Sheet 17	of 99



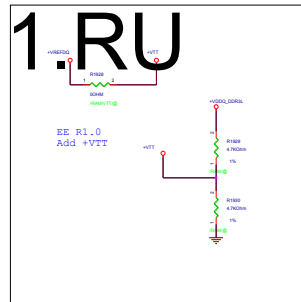
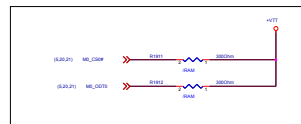
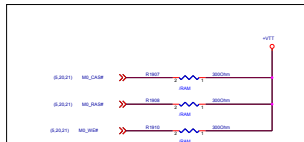
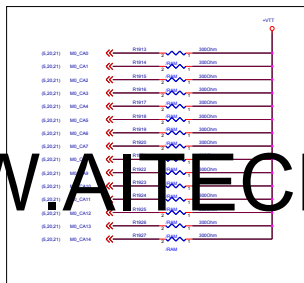
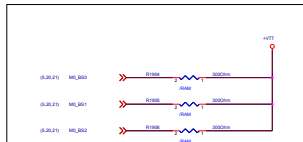
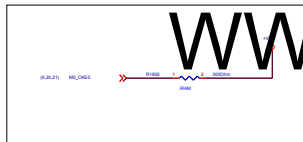
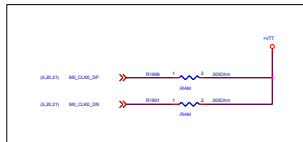
ER for EMI 0718



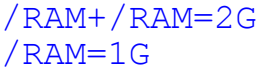
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/RAM=1G

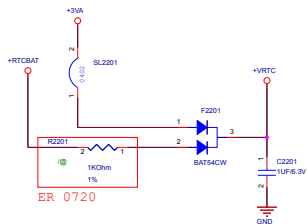
/RAM+/RAM=2G
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Termination

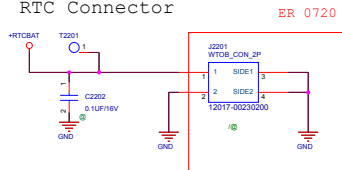


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RTC Connector

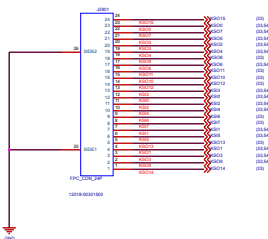


ER 不上RTC Conn 0720

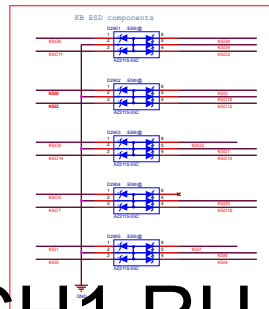
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ASUS		Title : RTC	
ASUSTek COMPUTER INC. EPAD		Engineer: EE3 RD	
Size	Project Name	Rev	
A4	X205TA	2.1	
Date: Thursday, December 18, 2014		Sheet	22 of 88

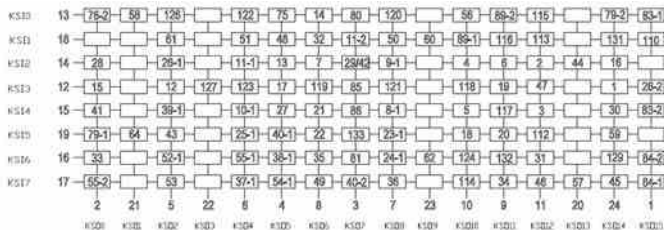
Keyboard



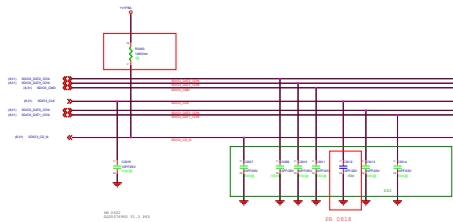
PR 0924 un-stuff for EMI



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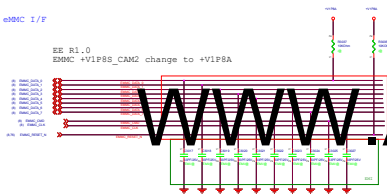


SD card I/F



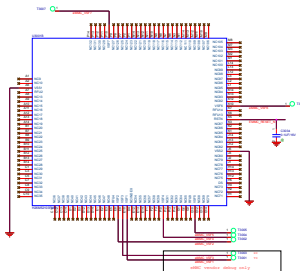
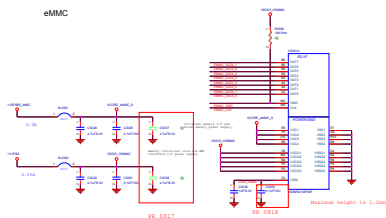
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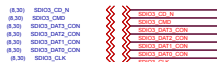
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EE R1.0
EMMC +V1P8S CAM2 change to +V1P8A
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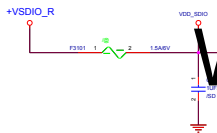
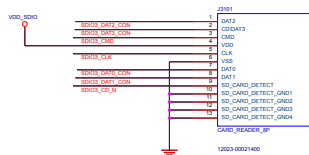
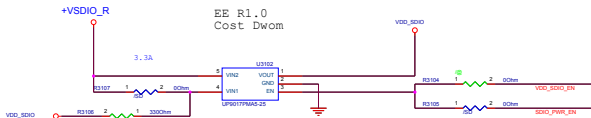
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eMMC

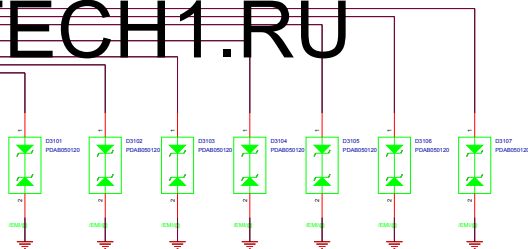
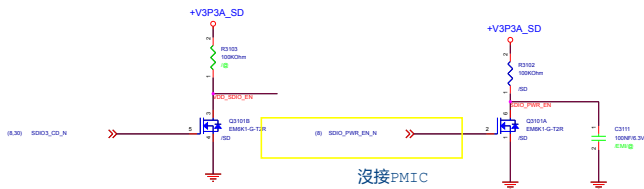




SD Card Connector



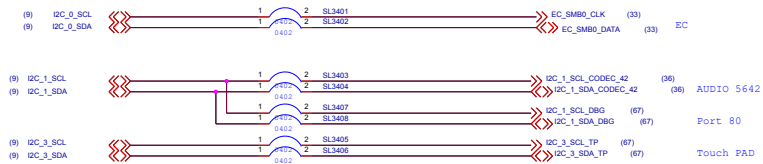
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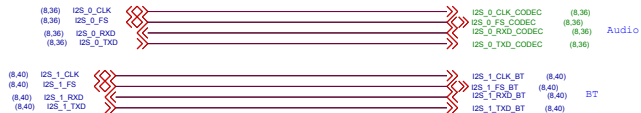
EE R1.0
ESD Diode

ASUS		Title : SD & VB & Hall CONN	
ASUSTAR COMPUTER INC. E990		Engineer: EE3 RD	
Size	Project Name	Rev	
B	X205TA	2.1	
Date	Thursday, December 18, 2014	Sheet	31 of 30

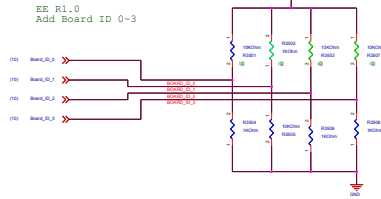
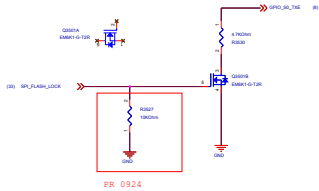




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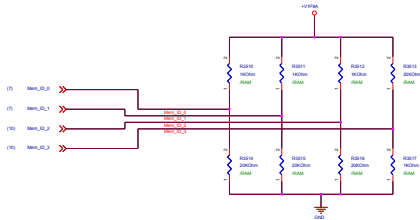


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ASUSTek COMPUTER INC. EPAD		Engineer: EE3 RD	
Size	Project Name	Rev	
A	X205TA	2.1	
Date:	Thursday, December 18, 2014	Sheet	34 of 99



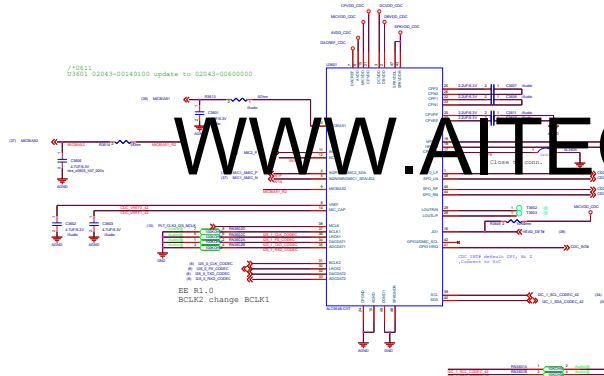
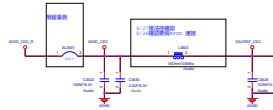
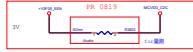
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0	0	0	1	SR-ST-001
0	0	1	0	SR-ST-002
0	0	1	1	SR-ST-003
0	1	0	0	SR-ST-004
0	1	0	1	SR-ST-005
0	1	1	0	SR-ST-006
0	1	1	1	SR-ST-007
1	0	0	0	SR-ST-008
1	0	0	1	SR-ST-009
1	0	1	0	SR-ST-010
1	0	1	1	SR-ST-011
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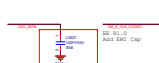
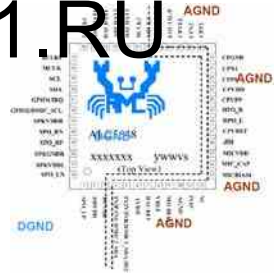


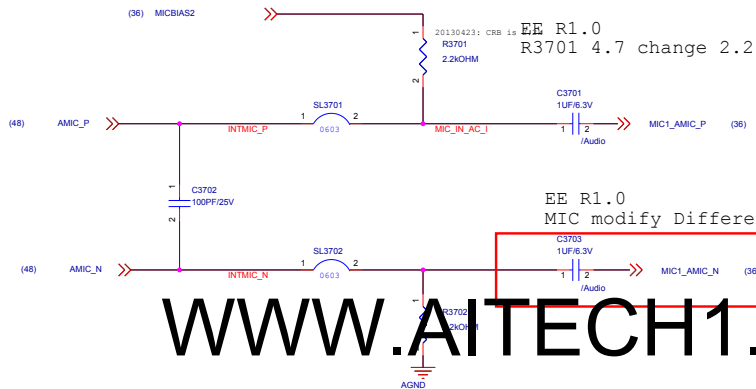
FR 0924 Add SAMSUNG Memory


MEM ID				
Mem_ID_3 (GPIO_S5P0E)	Mem_ID_2 (GPIO_S5P0E)	Mem_ID_1 (GPIO_S5P0E)	Mem_ID_0 (GPIO_S5P0E)	NOTE
0	0	0	0	0000-0000-0000-0000
0	0	0	1	0000-0000-0000-0001
0	0	1	0	0000-0000-0000-0010
0	0	1	1	0000-0000-0000-0011
0	1	0	0	0000-0000-0000-0100
0	1	0	1	0000-0000-0000-0101
0	1	1	0	0000-0000-0000-0110
0	1	1	1	0000-0000-0000-0111
1	0	0	0	0000-0000-0001-0000
1	0	0	1	0000-0000-0001-0001
1	0	1	0	0000-0000-0001-0010
1	0	1	1	0000-0000-0001-0011
1	1	0	0	0000-0000-0001-0100
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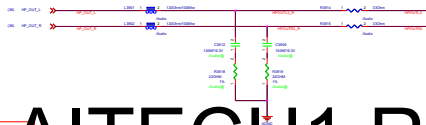
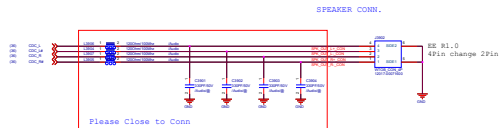


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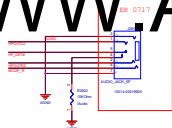




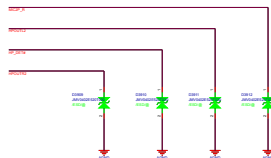
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ASUSTek COMPUTER INC. EPAD		Engineer:	EE3 RD	
Size A	Project Name X205TA			Rev 2.1
Date: Thursday, December 18, 2014		Sheet	37	of 99

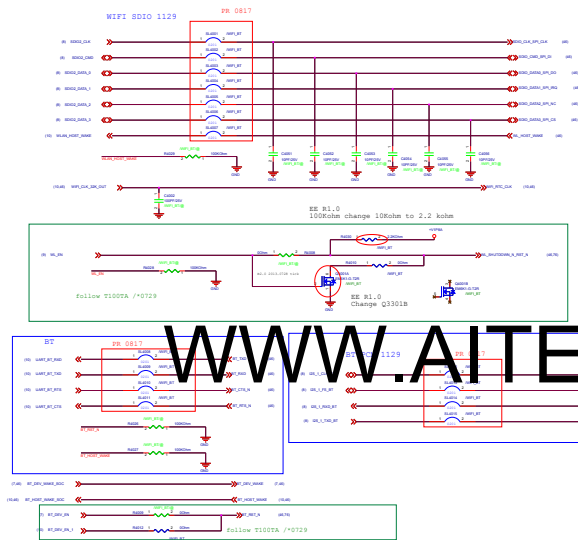


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2nd source
12014-00710100

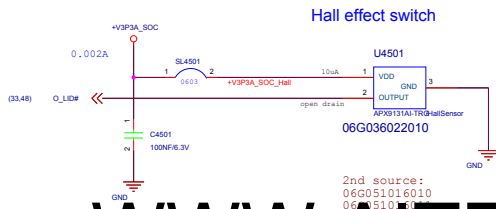




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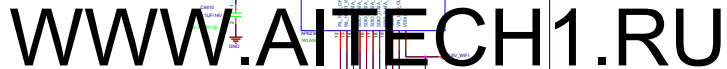
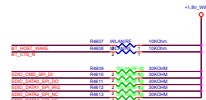
R4011, R4023, R4024, R4025, B=測試若沒問題, PR改版時請改成 Short Pin

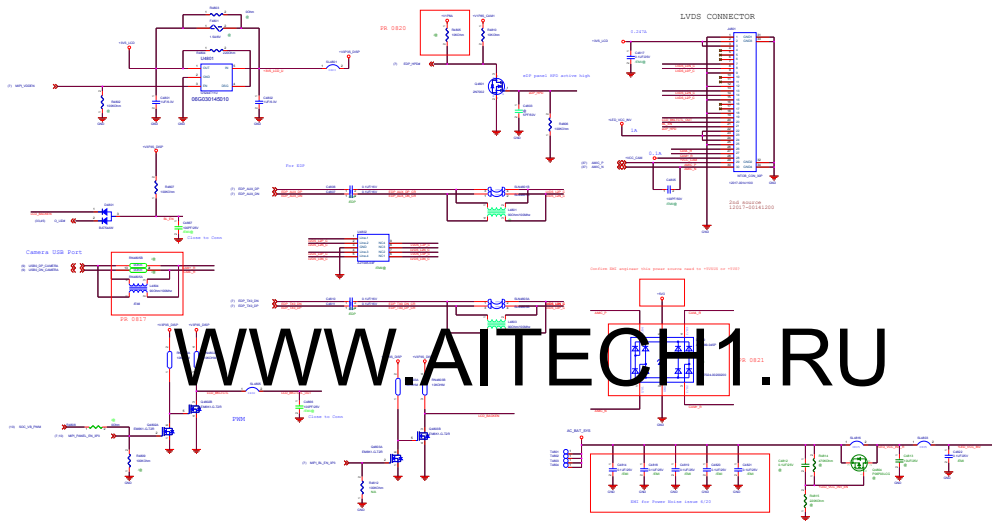
EE R1.0
Modify3P3A



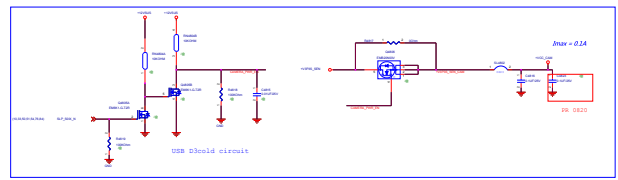
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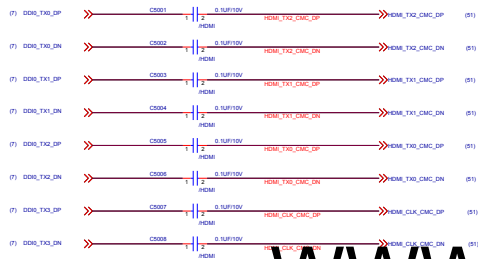
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ASUS		Engineer: EE3 RD	
ASUSTek COMPUTER INC. NB			
Size	Project Name	Rev	
A	X205TA	2.1	
Date: Thursday, December 18, 2014		Sheet	45 of 99



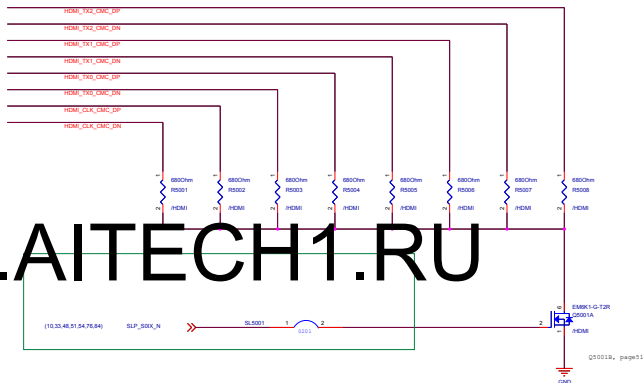


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WWW.AITECH1.RU

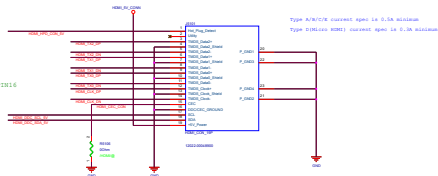


follow TI00TA /*0729

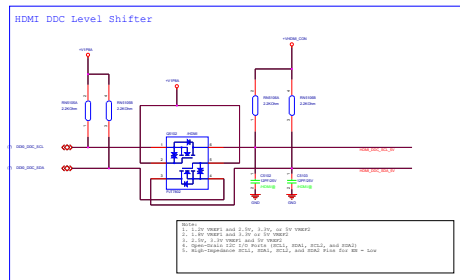
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ASUSTeK COMPUTER INC. NB		Engineer:	EE3 RD
Scale	Project Name	Rev	
B	X205TA	2.1	
Date: Thursday, December 18, 2014		Sheet	50 of 80

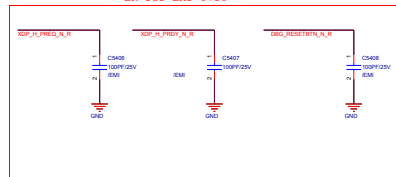
Micro HDMI Type Connector



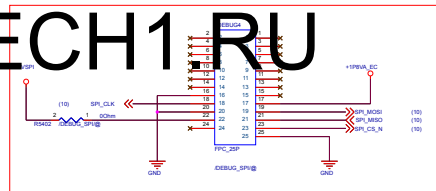
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ER for EMI 0718

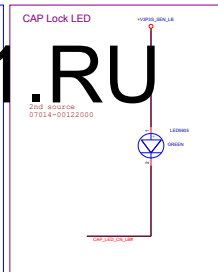
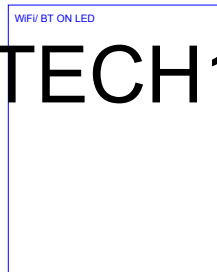
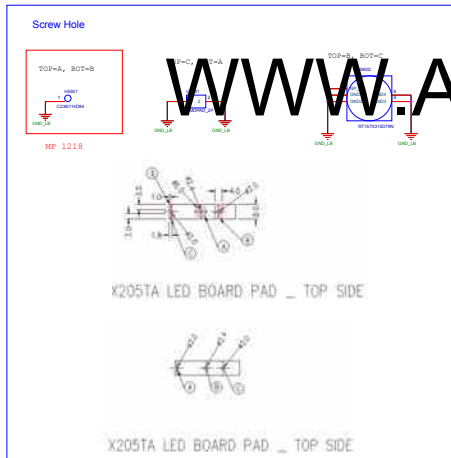
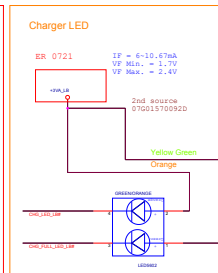
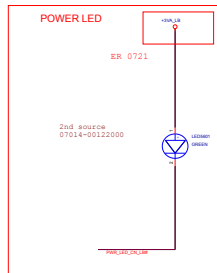
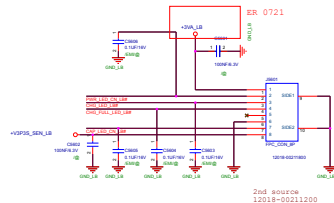


ER 0721



		Title : XDP_DEBUG	
ASUSÄTA COMPUTER INC		EE3 RD	
Size B	Project Name X205TA	Rev 2.1	
Date : Thursday, December 15, 2011		Sheet 54	of 95

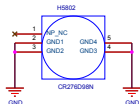
2014_1218



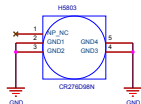
TOP=A, BOT=A



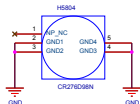
TOP=B, BOT=B



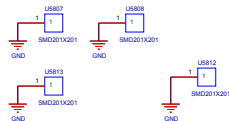
TOP=C, BOT=C



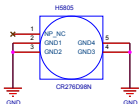
TOP=G, BOT=G



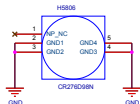
TOP=J, BOT=L



TOP=F, BOT=F



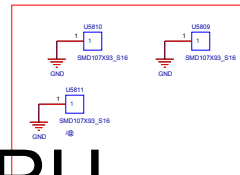
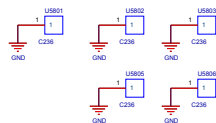
TOP=H, BOT=H



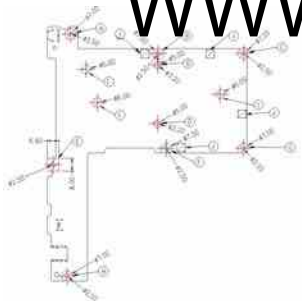
TOP=E, BOT=E



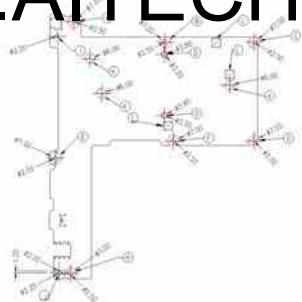
TOP=I, BOT=K



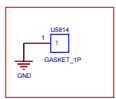
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X205TA MB SR TOP SIDE SCREW PAD



X205TA MB SR TOP SIDE SCREW PAD



PR for EMI 0819

定位孔

TOP=J, BOT=I



TOP=K, BOT=J

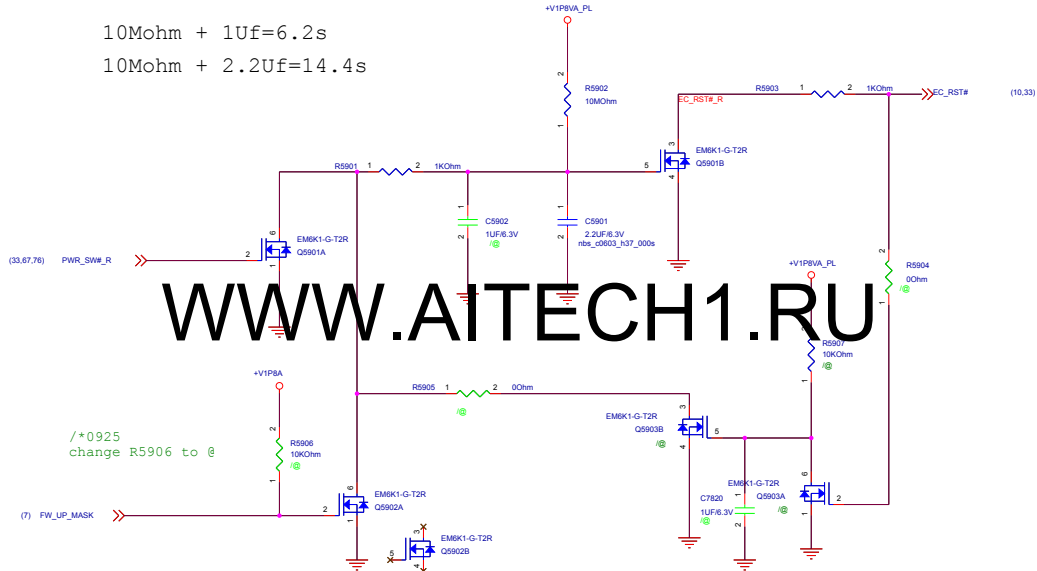


ASUS		Title : 58.Srew Hole	
ASUSTek COMPUTER INC. EAPD		Engineer: EE3 RD	
Size	Project Name	Rev	
A4	X205TA	2.1	
Date: Thursday, December 18, 2014		Sheet 08 of 09	

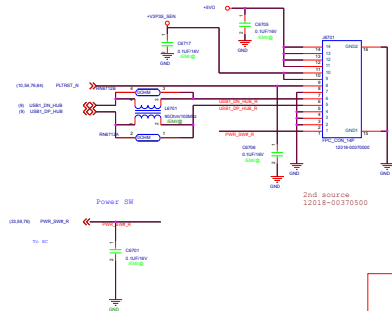
battery embedded (press pwr_sw 10sec, then reset ec)

$$10\text{Mohm} + 1\text{Uf}=6.2\text{s}$$

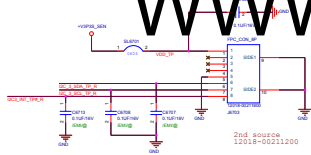
$$10\text{Mohm} + 2.2\text{Uf}=14.4\text{s}$$



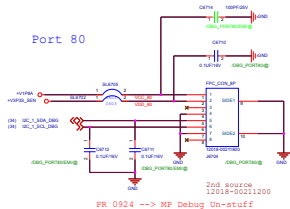
		Title 59.Power Sequnc Logic	
ASUSTek COMPUTER INC. EPAD		Engineer: EE3 RD	
Size A	Project Name X205TA		Rev 2.1
Date: Thursday, December 18, 2014		Sheet 59	of 99



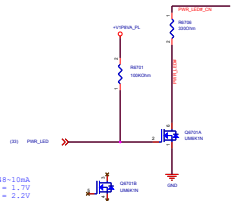
Touch PAD



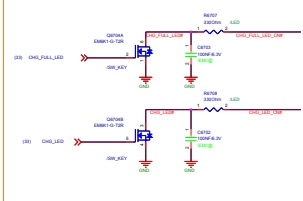
Port 80



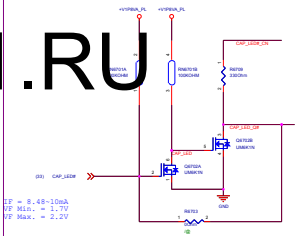
POWER LED



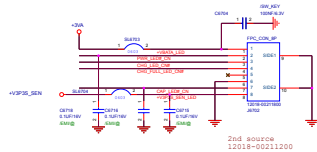
Charger LED



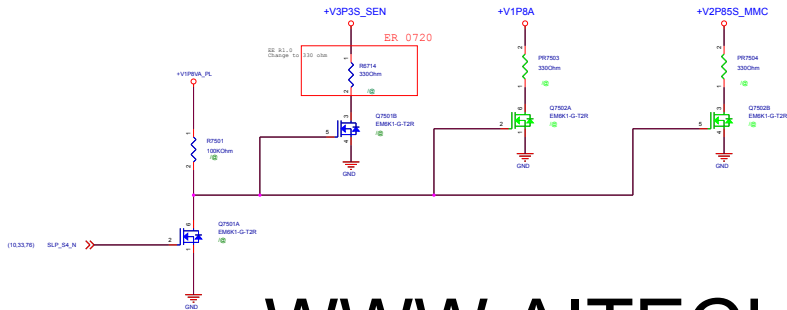
CAP Lock LED



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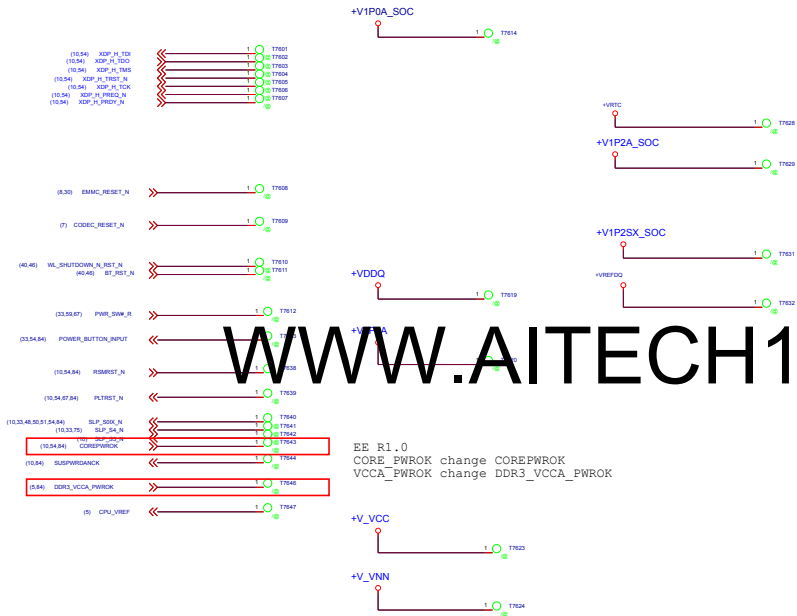


ASUS		Title : 87. B39 Conn	
ASUSTeK COMPUTER INC. CHN		Engineer: EE3 RD	
Model	Version	X205TA	Rev
A2			2.1
Date: Monday, December 18, 2017		Drawn	By: JF



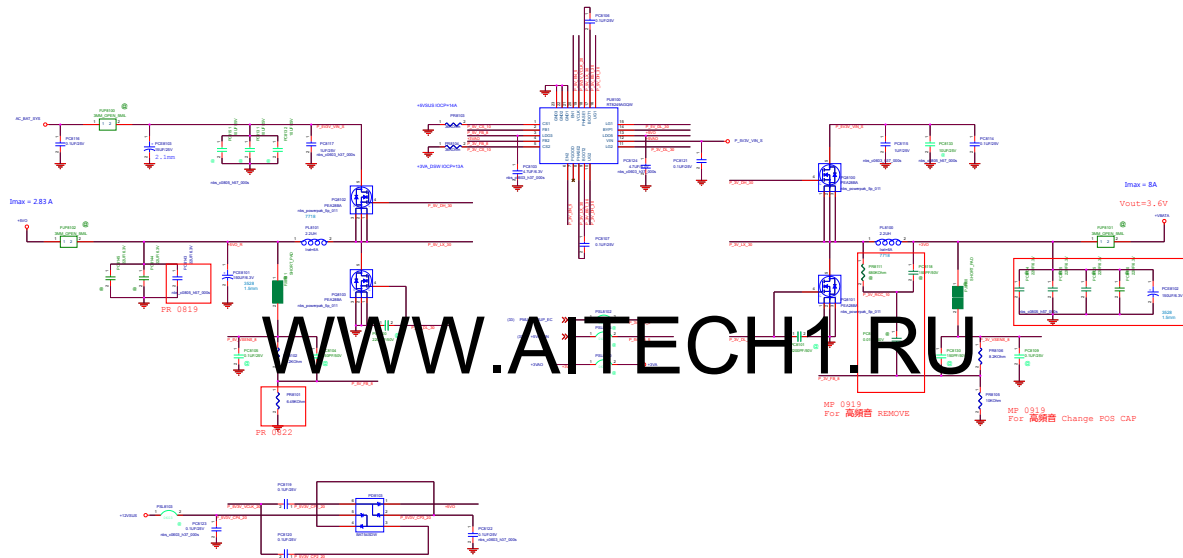
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ASUS		Title : 75.discharge	
ASUSTeK COMPUTER INC. EP4D		Engineer: EE3 RD	
Size	Project Name	Rev	
B	X205TA	2.1	
Date: Thursday, December 15, 2014		Sheet	15 of 50



EE R1.0
 CORE_PWROK change COREPWROK
 VCCA_PWROK change DDR3_VCCA_PWROK

+VBATA / +5VSUS [System Power]

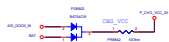
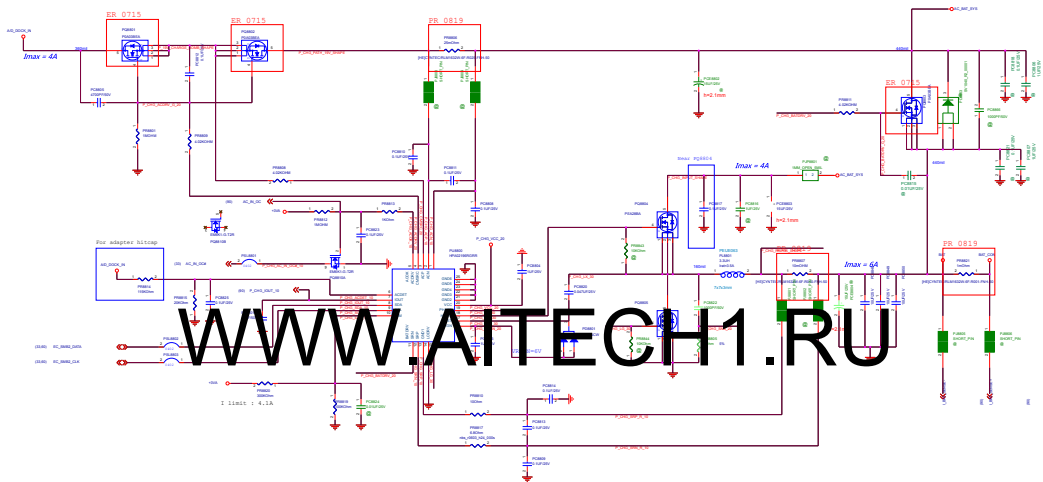


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請 check 墊料線路 +12VSUS 線路 並墊料的地點不得小於10.0mm

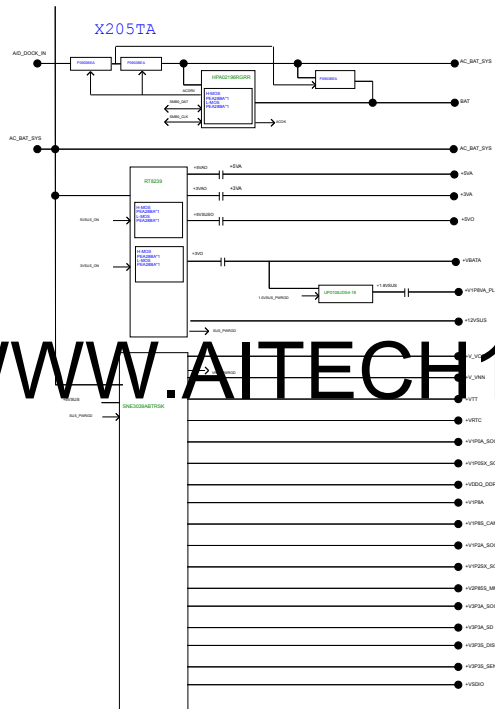
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		Project Name X205TA_Bay Trail-T CR	Rev 2.1
Title : +3VA_EC			
Size A4	Dept.: POWER		Engineer: Power
Date: Thursday December 18, 2014		Sheet 80	of 99



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